

711 PDT

The unlimited applications of the Daedalus Seven Eleven Programmable Data Terminal.



Anywhere there's a need for a terminal and better communications there's a need for a Daedalus Model 711.

Here are some applications to add to your own: centralized accounting from remote locations; centralized banking from branch offices; service bureaus, remember, because the 711 PDT is programmable service bureau clients would not have to conform to a centralized computer format which is often complex and repetitive; large corporations (e.g. public utilities, life insurance companies) could have more divisions, regional offices, distributors or dealers using their central processor; scientific computation and evaluation; inventory and production control; sales

analysis; daily, weekly, and monthly billings or profit; payrolls . . . and the list is practically endless.

Of course, you may not have to use our terminal for a terminal all the time.

You may wish to use it for a mini-minicomputer. Or use it like EAM equipment. Or use it for satellite equipment in the computer room.

Nationwide service.

Servicing Daedalus terminals is simple no matter where you locate them.

Thanks to Daedalus Service Centers.

The Centers strategically located within every industrial population area in the United States and Canada.

Which means we can promise you the fastest service possible.

Anywhere.

And we can also promise you the best service possible from factory-trained experts who know our terminals inside and out.

Experts that receive continuous training from us, maintain local parts inventories for you, and offer a fixed-cost or time and material service contract.

Specifications.

Chances are, you have engineers, programmers or systems men who want to know more about the specifications of our machine than you do.

And so we dedicated this whole page to them.

DUAL MAGNETIC CASSETTE TAPE TRANSPORTS

Characteristics	Phillips type cassette with computer grade tape recorded at 533 bits/inch for 300 feet.
Data Transfer Rate	Greater than 7000 bits/sec.
Input Code	8 level USASCII plus hardware parity bit.
Data Capacity	Appr. 125,000 characters per tape based on 128 character per block.
Block Size	Variable up to 256 characters.

KEYBOARD INPUT

Numeric Keypad

Method of Entry	Via 12 keys of Keyboard. This keyboard is arranged in the standard adding machine configuration.
Data Capacity	Up to 256 characters can be entered thru a single keyboard instruction under stored program control.
Character Set	12 distinct character codes, including 10 numerics; plus sign; and minus sign.

Alpha-Numeric Keyboard:

Method of Entry	Via 51 keys of keyboard. This keyboard is arranged in the standard typewriter configuration.
Data Capacity	Up to 256 characters can be entered thru a single keyboard instruction under program control.
Character Set	59 distinct character codes, including numeric; upper-case alphabets, punctuation; and special symbols.

Function Keygroup:

Method of Entry	Via 8 keys of keygroup. The keys in this keygroup are arranged 2 x 4 and can be used to enter a transaction code and terminate a keyboard entry instruction under stored program control.
Character Set	8 Distinct character codes, all numeric.

OPERATING PROCEDURE

Attended Operation	Before a message is transmitted, predetermined programs and time of transmission should be established between the communicating terminals. Programs should be on program tapes and ready for immediate use.
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Unattended Operation

Remote terminals are left in a ready status with programs loaded, tape cassettes loaded, and waiting to respond to a signal from the computer center and then the data tape from the remote unattended terminal would be transmitted for batch processing.

PRINTER

30 cps, 64 printable characters.

Paper Forms

Pin-fed fanfold multi-part forms up to 14⁷/₈ inches wide with 132 print positions.

Format Control

Under program control or incoming data or manually by operator. Controls include line feed, carriage return, backspace and home paper. Formatting under program control can include such things as zero suppression and other logical functions.

MEMORY

The core memory of 512 bytes is used for storage of both program and data information with a memory cycle time of 2 microseconds. The memory may be expanded in multiples of 512 bytes.

UNIVERSAL I/O CHANNEL

This allows user to interface up to eight external peripheral devices each individually addressable by programming. Daedalus supplies the most common interfaces.

MODEM

This unit consists of all circuitry necessary to interface between Daedalus terminals and a telephone line coupler. Data transfer rate is 1200 baud. Average error rate is less than 1 character per 100,000 characters transmitted.

Rated Transmission Speed

1200 baud.

Effective Data Rate

100 Characters per second.

Transmission Method

Serial by bit.

Transmission Code

8-Level USASCII plus SYNC bit.

Transmission Mode

Half-Duplex—Synchronous.

Order of Bit Transmission

Low order data bit first.

Mode of Operation

Attended or unattended.

CONNECTION TO COMMUNICATIONS LINES

Public Telephone Network Operating at 1200 baud

Standard Telephone Company manual or automatic data access arrangement. Daedalus supplies the modem as standard equipment.

Dimensions

Length—55"
Width—31"
Desk Height—26¹/₄"
Total Height—37¹/₄"

Weight

400 pounds

Voltage Requirements

110 A.C., 5 amps, 60 Hz

Daedalus products are constantly improving. Hence, specifications are subject to change without notice.

Instructions.

The following instruction repertoire is the main reason why your programmer is going to like the truly programmable Model 711 Daedalus Terminal.

But there are other reasons too.

One's called "Daedatran." Which is our symbolic programming language for writing programs that are to be executed on our terminal. Write a program in this language and it can be translated in this terminal.

The translated program is written out on the cassette tape, stored and used when needed. Or mailed and used where needed.

Another reason why your programmer is going to like our terminal is because it's easy to program.

And here is the main reason spelled out:

SET ADDRESS INSTRUCTIONS

SPI — Set Page Instruction
SPA — Set Page Address A
SPB — Set Page Address B
SAA — Set Address A
SAB — Set Address B

JUMP INSTRUCTIONS

JPU — Jump Unconditionally
JER — Jump on Error
JPE — Jump on Equal
JPL — Jump on Less
JPG — Jump on Greater
JPS — Jump Store

ADDRESS MODIFICATION INSTRUCTIONS

MAD — Modify Address
IAA — Increment Address A
IAB — Increment Address B

DATA MANIPULATION INSTRUCTIONS

CHK — Check
MVC — Move Characters
ADS — Add Signed
ADU — Add Unsigned
NTC — Number To Complement
CTM — Complement To Magnitude
CPC — Compare Characters
SFN — Scan For Numeric
PCK — Pack Record
UPK — Unpack Record

PRINTER INSTRUCTIONS

PRC — Print Characters
PRL — Printer Space Line
PRB — Print Blanks
PRE — Printer Eject

KEYBOARD INSTRUCTIONS

KBL — Key Entry Left Justified
KBR — Key Entry Right Justified

CASSETTE TAPE INSTRUCTIONS

TPL — Tape To Load Point
TPB — Tape Back Space Record
TPW — Tape Write
TPR — Tape Read
TPS — Tape Search & Load of Program

COMMON INTERFACE INSTRUCTIONS

SEL — Select Common I/O Channel
CIA — Common Interface Control A
CIB — Common Interface Control B
CIC — Common Interface Control C
CIR — Common Interface Read
CIW — Common Interface Write

DATA COMMUNICATION INSTRUCTIONS

DCA — Data Communication Control A
DCC — Data Communication Control C
DCR — Data Communication Receive
DCT — Data Communication Transmit

PROGRAM CONTROL INSTRUCTIONS

HLT — Halt
HLC — Halt on Absence of Carrier

PSEUDO INSTRUCTIONS

BGN — Used to assign program ID to translated program on tape.
HDG — Used to generate a heading line on the program listing.
COM — Used to generate remarks on the program listing.
BCD — Used to enter alpha/numeric literals into program.
BIN — Used to enter non-keyboard characters into program.
ORG — Controls memory assignment with new address.
OVL — Used to set instruction address of program overlays.
END — Used to indicate end of program to translator.

Software support.

We've got plenty of it.

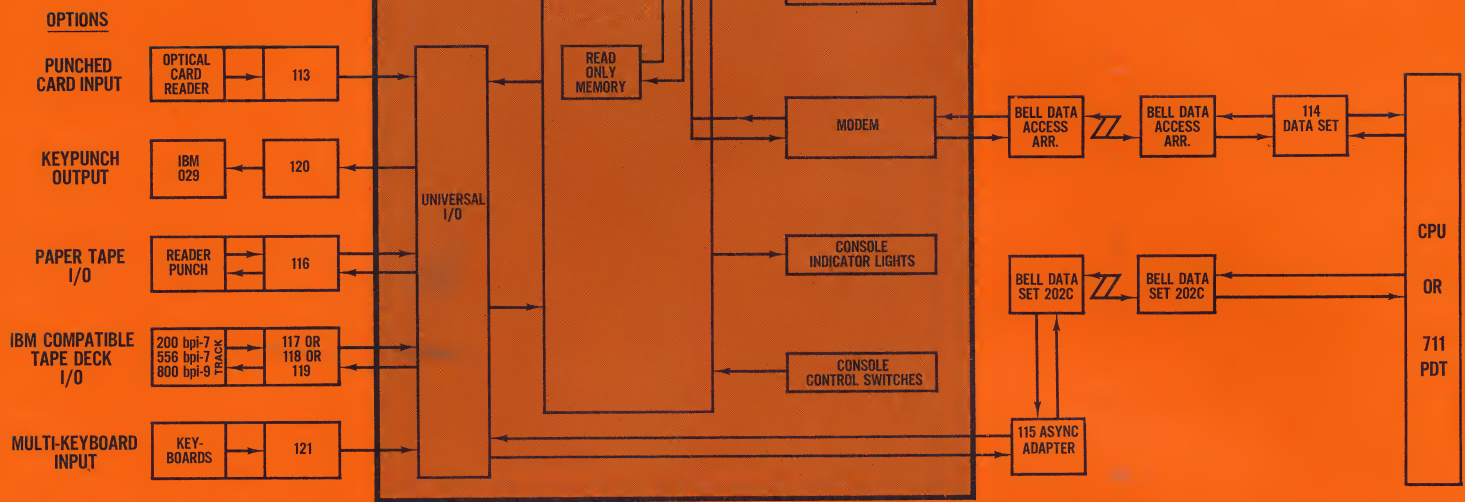
Which makes sense in case you don't have the support you need.

We have knowledgeable, experienced people who know how to solve applications with our terminals.

And an easy-to-understand Programming Manual for your programmers.

So if you think software is going to be a problem, forget it.

711 PDT



Optional accessories.

Flexibility is built into the Model 711 Programmable Data Terminal.

Amazingly.

To start, our 113 provides for punched card input from a 400 cpm optical card reader.

Our 120 provides an output interface with your IBM keypunch.

Our 116, with our reader/punch gives you paper tape I/O abilities.

And the Daedalus 117, 118 and 119, each of which is supplied with an IBM compatible tape deck, are the I/O interfaces with either 200 bpi and 556 bpi 7-track tape or 800 bpi 9-track tape.

The 114 data set, with a standard RS-232 interface, lets you transmit and receive in a computer-compatible language at 100 cps.

The Daedalus 115 interface allows you to interface with a Bell Telephone 202C data set.

And for multi-keyboard input, our 121 is the interface required.

When we built the 711 Programmable Data Terminal we made sure it would fit into your plans, system and budget.

Without squeezing.

Prices and deliveries.

The average purchase price of a Model 711 Programmable Data Terminal is under \$12,500. As is the nature of our industry, quantity discounts apply.

So let us know exactly how many units you'll need and we'll let you know exactly what they will cost. Instantly.

The same holds true for our lease/rental programs. Please tell us or a Daedalus District Sales Representative how many terminals you require, how long you want them and we'll respond immediately.

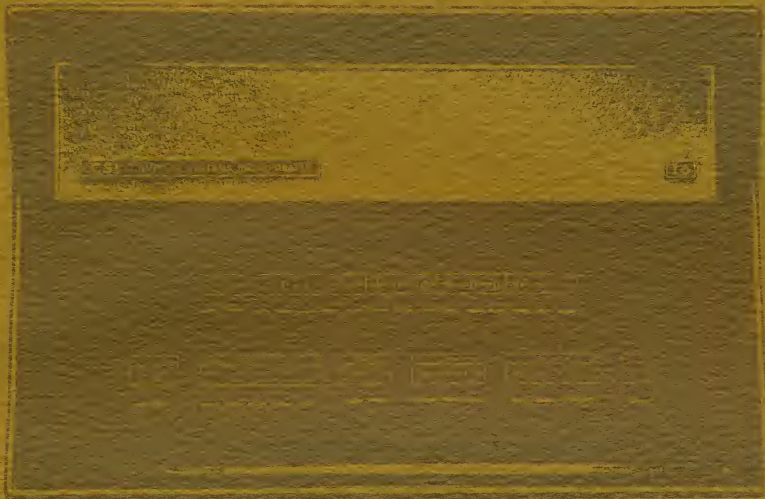
You won't have to wait until then to find out our product is available now and that we can begin to deliver eighty days after we receive your order.

For additional product and pricing information, and to arrange for an appointment with your nearest Daedalus District Sales Representative, please contact:

Daedalus Computer Products, Inc.
P.O. Box 248
North Syracuse, New York 13212
(315) 699-2631

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HARDWARE

Memory CSI 16 — up to 32,768 16-bit words
 CSI 24 — up to 8,388,608 24-bit words
 Cycle Time — 900 nanoseconds

Seven Instruction Processor registers including three double word Accumulator/Buffers, Memory Protection, Program Relocation, Index and Instruction Counter registers

Integer add, subtract, multiply and divide hardware

Floating Point add, subtract, multiply and divide hardware

Interrupt system that provides up to 256 priority interrupt levels

1.1 million word per second Direct Memory Access Input/Output controlled by up to 256 independent I/O Processors, each capable of controlling up to 256 Device Processors

SOFTWARE

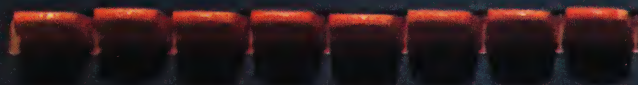
One-pass Assembler operable in 4,096 words of memory

One-pass Extended ALGOL, BASIC or ASA FORTRAN IV Compiler operable in 4,096 words of memory

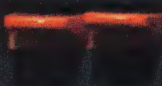
Four operating systems to meet diverse needs

CSI COMPILER SYSTEMS INCORPORATED

31 | 15 30 | 14 29 | 13 28 | 12 27 | 11 26 | 10 25 | 09 24 | 08



HIGH	LOW
31 16	15 00



REGISTER				
A	X	I	R	P



MEMORY	
FETCH	STORE



16

23|07 22|06 21|05 20|04 19|03 18|02 17|01 16|00

CLOCK
ENABLE INHIBIT PULSE

EXECUTION
RUN HALT RESET START

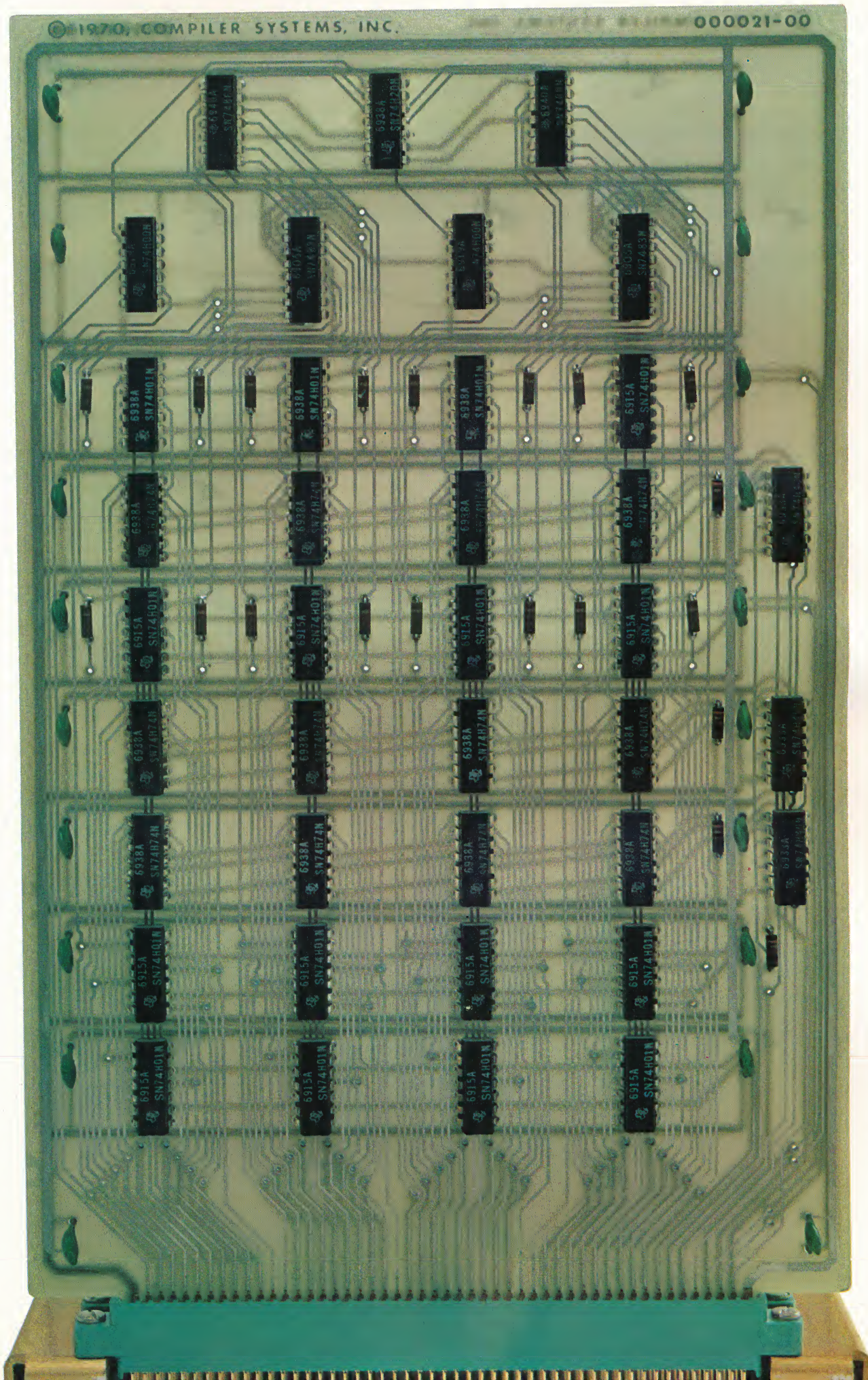
POWER

THE SYSTEMS

The architecture of presently available computer systems does not interface well with the requirements of high level compiler languages. Utilizing high level languages, the systems produce programs that require significantly greater memory capacity and more time to execute than comparable programs written in assembly language. Therefore, if speed and efficiency are considerations, many expensive man-hours are required to write the programs, and generally the skill of an experienced programmer with knowledge of the specific computer being used is also required. Hardware costs are decreasing, but because of system architectural problems, software costs are rapidly increasing.

The CSI 16 and CSI 24 computer systems reduce software costs by obviating the necessity of programming in assembly language. They represent a new concept in computer design in that the software requirements, efficient operation in compiler language environments, were defined; then the hardware was designed to interface with those requirements. The hardware/software architecture allows the user to direct his efforts to the specific task to be performed utilizing a machine independent language. The user, therefore, is freed to concentrate on the application of the computer system and not the computer system itself.

Data Processing problems, large or small, are handled with equal ease by the systems. Their architecture is analogous to that of very large machines. Powerful, efficient compilers and instructions and high speed floating point hardware give the systems "number crunching" capability found only in very large, expensive systems. In addition, all Input/Output is controlled by I/O Processors which are independent of Instruction Processor operations, freeing the Instruction Processor for high priority computing tasks.



INSTRUCTION PROCESSOR

The cost/performance ratio of the CSI systems is virtually unparalleled. Their exceptional computing power is several times greater than that of comparably priced systems while systems of comparable performance are several times more expensive.

The basis for this capability is the architecture of the Instruction Processor. Use of efficient algorithms has greatly simplified the architecture resulting in optimum utilization of a minimum amount of hardware.

Hardware algorithms are provided for the basic compiler language functions, providing efficient integration with the high level language software requirements, thus, attaining optimum program efficiency.

Total system efficiency is generally characterized by throughput speed which is dependent on hardware speed and program size, and the time required to program the system. The CSI systems optimize throughput with high speed logic and arithmetic circuits, and efficient operation in compiler language environments.

REGISTERS

ACCUMULATOR REGISTER (A). The double word Accumulator register temporarily stores the results of arithmetic operations which occur in the Buffer registers B and C. For integer operations, the lower word is used; and for real operations, both words are used. High speed

shift and pack instructions provide data packing and field manipulation capability. Data conversion from integer to real and from real to integer is also accomplished in the Accumulator register.

BUFFER REGISTERS (B) AND (C) These two double word general purpose registers, in conjunction with the adders, perform all of the arithmetic and address calculations.

INDEX REGISTER (X). This register is used primarily for referencing arrays. To facilitate index calculations, integer arithmetic and test operations are performed in this register without disturbing the Accumulator register. When referencing real arrays, the hardware address computation automatically doubles the contents of the Index register to allow for the double word length of real numbers. The Index register is also used for setting up input/output transfers, program initiation, interrupt control and counting iterations for the shift instructions.

INSTRUCTION COUNTER (I). This register contains the address of the instruction to be executed. After the instruction is executed, the Instruction Counter is incremented and contains the address of the next instruction.

RELOCATION REGISTER (R). This register enables a program compiled to run in a particular memory location to run in different memory locations without program loading delays for address modification. For a given program, the Relocation register points to the last word

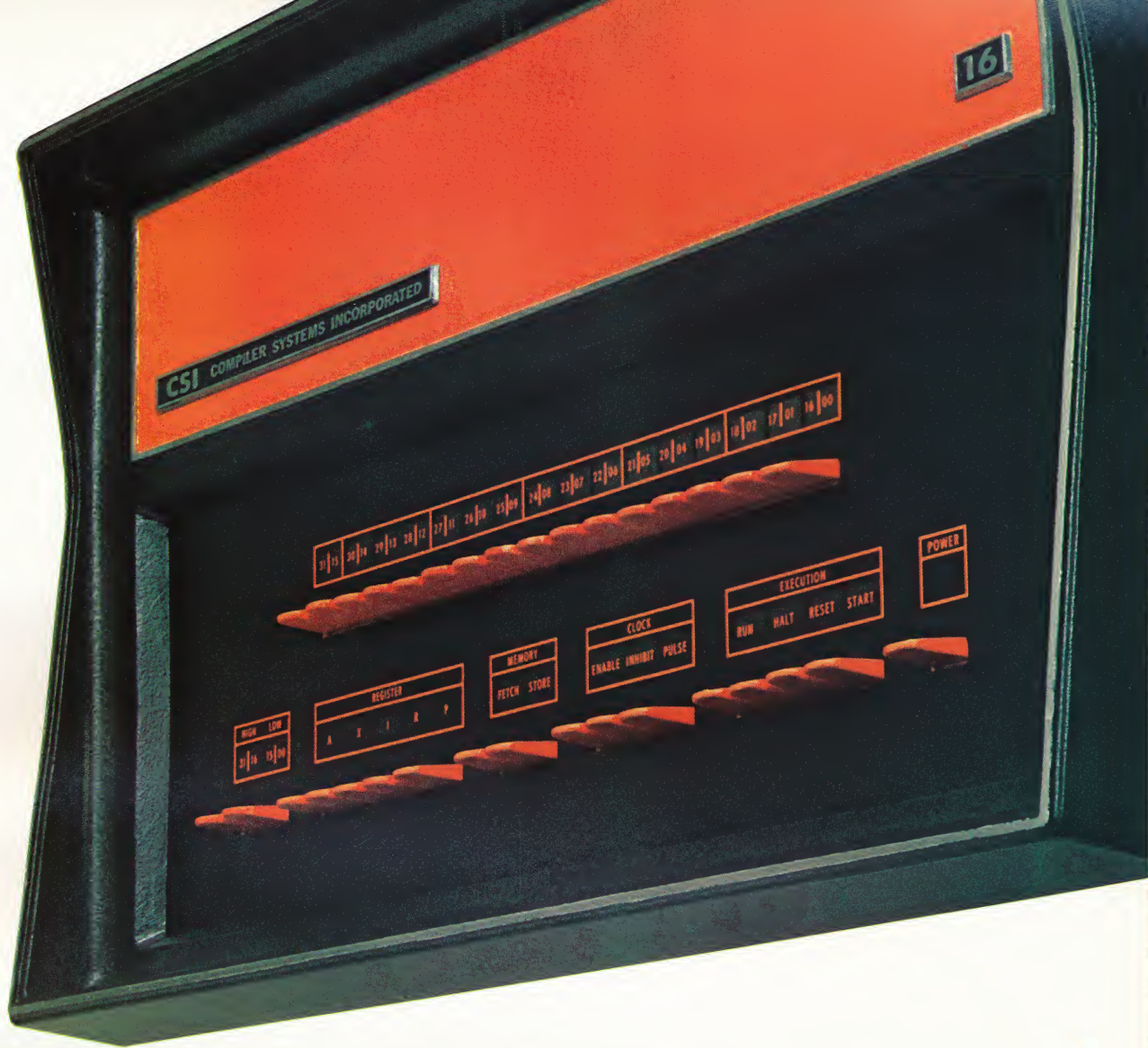
in the program. All addressing within the program is accomplished by calculating offsets from this point. The address calculation is accomplished by the hardware and does not increase execution time. The Relocation register also serves as the base boundary for memory protection.

PROTECTION REGISTER (P). This register specifies the end of a variable length address field in which a program is restricted. The Protection and Relocation registers specify the boundaries to be protected by the memory protection hardware. This protects inactive core-resident programs by preventing the program operating within the boundaries from referencing addresses in the protected area outside the boundaries. As priorities and active programs change, the operating systems make fast, dynamic changes to the protection boundaries.

ITYPE REGISTER. A 1-bit register set by the Fetch instructions that specifies whether arithmetic operations are to be integer or real (fixed point or floating point).

IREG REGISTER. A 1-bit register set by the Fetch instructions that specifies whether arithmetic operations are for the Accumulator or the Index register. It is set to index after each store instruction in anticipation that the next instruction will involve an index operation.

OPERATION CODE REGISTER (OPC). The Operation Code register temporarily stores the op-code of each instruction word. The contents of the register specify the operation to be executed.



MEMORY

The basic computer systems include a 900 nanosecond cycle time memory module of 4,096 16 or 24-bit words. The CSI 16 memory is expandable in increments of 4,096 words to a maximum of 32,768 words, all in the mainframe. The CSI 24 memory is expandable in increments of 4,096 words to 32,768 words in the mainframe and is expandable to a maximum of 8,388,608 words through the use of optional memory extension systems.

The Memory is accessible from two sources; the Instruction Processor and the Input/Output Processors. Multiplexer control circuits in the Instruction Processor allow the Memory to be shared on a cycle stealing basis with the I/O Processors having priority over the Instruction Processor.

Large capacity, rapid access, relatively low-cost memory devices are presently under development in the industry. The ability of the CSI 24 to address 8,388,608 words of memory, and the Instruction Processor's independence of memory speed, will enable the user to take full advantage of these new devices as they become available.

INTERRUPT SYSTEM

True real-time interrupt response is provided by the priority interrupt system. The basic system consists of 4 levels of priority interrupt with the capability of being expanded to 256 levels in modular increments of 4. The system automatically identifies and ranks each individual interrupt in hardware. Response time to an interrupt, including context switching, is 6.3 microseconds. Upon receipt of a higher priority interrupt, the hardware automatically stores the registers of the current program and control is transferred to the new interrupt routine. Upon completion of the routine, a single instruction restores the registers and returns control to the interrupted program. All interrupt control can be accomplished through the use of high level compiler language statements.

INPUT/OUTPUT PROCESSORS

The power and flexibility of the CSI I/O system is found only in very large, expensive computer systems. A data transfer rate of up to 1.1 million words per second is provided via a Direct Memory Access

channel controlled by independent I/O Processors. These processors are micro-programmed hardware computers designed specifically for the task of I/O processing. Each processor consists of a List Address, Data Address, Data and Data Count registers and hardware control algorithms. Initiation of an I/O transfer is accomplished by one instruction from the Instruction Processor to the appropriate I/O Processor. Data is transferred on a record basis, the record size being a function of both the program and the data transmitted.

The computer system's multi-processor configuration allows data transfer operations to occur simultaneously with the operation of the Instruction Processor without interrupting the program. This is accomplished by allowing the I/O Processors and the Instruction Processor to share the memory on a cycle stealing basis; however, I/O Processor memory requests have priority over Instruction Processor memory requests.

The system accommodates up to 256 Processors requesting memory cycles simultaneously, the requests being granted on a hardware priority basis. Each Processor has the capability to control up to 256 devices asynchronously.

Available devices include the following:

Teletype and Typewriter Terminals

Paper Tape Punch and Reader

Card Punch and Reader

Line Printer

Cassette Magnetic Tape

High Speed Magnetic Tape

Disk Memory

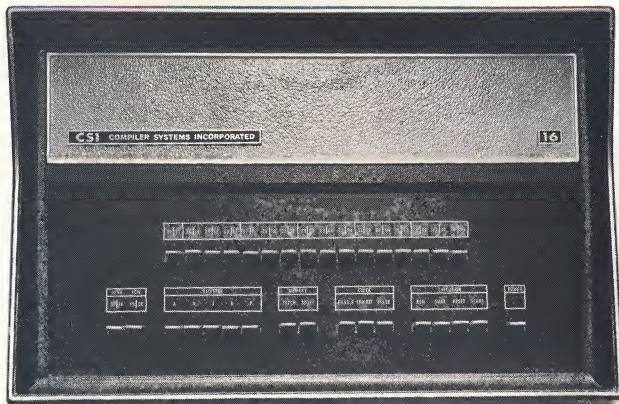
Graphic Plotters and Displays

Data Acquisition and Control Systems

Data Communications Systems

PERIPHERAL DEVICES

Peripheral devices are available for a large variety of system configurations. Modular expansion capability allows a minimum system to be easily expanded to meet current or future requirements.



SPEED AND EFFICIENCY/EXAMPLES

FORTRAN

The CSI system execution time for the following typical FORTRAN do-loop (including loop initiation, one hundred passes and loop termination) is less than

4 milliseconds. The major reasons for the short execution time are floating point hardware, powerful indexing capability, and compact compiler generated object code.

```

      Real F(100), G(10, 100), H(100)
      Do 200 I = 1, 100
200    F(I) = G(J,I) * H(I)
  
```

The CSI compiler generates the following code:

LINE NO.	LABEL	OP CODE	OPERAND	COMMENT
1		FXI	= 1	First index for do-loop
2	\$ 1M	STO	I	Set I
3		MUL	= 10	Compute G index where
4		ADD	J	Index = 10*I + J
5		*FAR	= *G-11	Fetch G array value
6		FXI	I	Restore Index with I
7		*MUL	= *H-1	Multiply Accumulator by H value
8		*STO	= *F-1	Store produce in F
9		ADD	= 1	Increment Index
10		TGT	= 100	Test for end of loop
11		BRA	\$ 1M	Loop incomplete — loop

EXPLANATION:

Lines 3 and 4 illustrate the ability to do arithmetic calculations in the Index register. The index calculated is the actual element number within the G array. The hardware realizes in line 5 that the Fetch involves a real array, and automatically doubles the Index for the address calculation.

Line 6 restores the Index register, but the following line refers to the Accumulator

register as required because all indexed instructions except FXI refer to the Accumulator register

Lines 9 and 10 refer to the Index register because the STORE instruction in line 8 sets a bit that causes the next instruction to be an Index operation unless that instruction indicates otherwise.

MATH ROUTINES

Function	Definition	Name	Program Size (Words)	Execution Speed (in microseconds)	
				CSI-16	CSI-24
Exponential	e^a	EXP	73	166	202
Natural Logarithm	$\log_e(a)$	ALOG	66	148	175
Common Log	$\log_{10}(a)$	ALOG10	67	152	170
Trigonometric Sine	Sin(a)	SIN	80	145	167
Trigonometric Cosine	Cos(a)	COS		149	172
Hyperbolic Tangent	Tanh(a)	TANH	25	223	268
Square Root	$(a)^{1/2}$	SQRT	43	158	185
Arctangent	Arctan(a)	ATAN	66	165	201



COMPILER SYSTEMS INCORPORATED

Eastern Region
P.O. Box 366
Ridgefield, Connecticut 06877
(203) 438-0488

Western Region
P.O. Box 269
San Rafael, California 94902
(415) 479-8442